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EXAMINER
ZALEPA, GEORGE D

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/685,501	Applicant(s) SMITH, GRAEME ROY	
	Examiner George D. Zalepa	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/29/05, 10/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-45 have been considered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Reconfigurable integrated circuit utilizing controller elements and processing elements of differing architectures and real time and non-real time configurable interconnect.

Claim Objections

3. Claims 15, 22, 31, 35 and 40-42 is objected to because of the following informalities: In lines 2, 2, 3, 4, 2, 2, and 2 of claims 15, 22, 31, 35, 40, 41, and 42 (respectively) all contain an inappropriate use of a period within a sentence. Furthermore, claim 34 recites the term "controller element" which is inconsistent with the remained of the claim; the examiner gives the suggestion, "controller elements". Appropriate correction is required.

4. Claim 42 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 42 depends on claim 40 which recites the same limitation.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 9, 11-13, 33, 34 are rejected under 35 U.S.C. 102(b) as being anticipated by DeHon et al (US Pat. 5,956,518).

7. Regarding **independent claim 1,**

8. DeHon discloses *a reconfigurable integrated circuit* [see DeHon, Col. 2, lines 15-20] *comprising a plurality of controller elements, the plurality of controller elements including a first controller element and a second controller element* [see DeHon, Figs. 1-5, elements F, A, B; Col. 5, lines 16-21], *the first controller element having a certain architecture and a second controller element having a certain architecture, the first architecture being different from the second architecture* [see DeHon, Col. 11, lines 45-49; Col. 12, lines 9-12 and 20-25 (description of real-time programmable control architectures); Col. 13, lines 38-40; lines 44-47 (description of a hardwired control architecture); Examiner's note: In the aforementioned citations, DeHon discloses two different control schemas are given for control structures. The first (Col. 11, lines 45-49; Col. 12, lines 9-12 and 20-25) describes a dynamic control system wherein user-defined control structures are selected to be used for implementing a control unit. The second (Col. 13, lines 38-40; lines 44-47) describes the use of a hard-wired controlling mechanism which is unable to be defined by a user. Thus, DeHon discloses two different control architectures.]; *a plurality of processing elements, the plurality of processing elements including a first processing element and a second processing element* [see DeHon, Fig. 4, elements "ALU" etc.], *the first processing element having a certain architecture and a second processing element having a certain architecture, the first architecture being different from the second architecture* [see DeHon, Col. 2, lines 28-34; lines 43-47; Examiner's note: Lines 43-47 defines an element that is constructed from multiple BFUs which is a different architecture when compared to a BFU that is independent and able to be independently changed. Furthermore, in Fig. 35, DeHon shows a plurality of functional units (elements 512, 514, and 516) being hardwired to perform either multiply or add functions, thus defining a rigid architecture. However, in Figs. 1-5, DeHon discloses an "ALU" which is routinely configured to perform different operations,

similar in spirit to an ALU in a modern processor, which is dynamically configured to perform operations dependent on an instruction being processed. These two different architectures thus define two distinct architectures being utilized within the invention disclosed by DeHon.]; *and reconfigurable interconnection means* [see DeHon, Col. 2, lines 6-10; Col. 8, lines 18-21], *which can be configured by one or a plurality of controller elements, the reconfigurable interconnection means being dynamically reconfigurable in real time* [see DeHon, Col. 12, lines 7-15; Examiner's note: In this passage, DeHon describes the BFUs reconfiguring each other dynamically, thus in real time.] *and non real time* [see DeHon, Col. 13, lines 43-47; Examiner's note: In this passage, DeHon discloses a plurality of connections be configured, such as in a startup mode, thus not in real time.], *the reconfigurable interconnection means allowing data transfers between processing elements* [see DeHon, Fig. 3, connections between ALUs] *and data transfers between processing elements and controller elements* [see DeHon, Fig. 3, connections between F, A, B, and ALUs].

9. Regarding **claim 2**,

10. DeHon discloses *the reconfigurable integrated circuit of claim 1, wherein the first controller element architecture and the second controller element architecture are selected from a plurality of specific architectures, the plurality of architectures including rigid architectures and programmable-rigid architectures* [see DeHon, Col. 11, lines 45-49; Col. 12, lines 9-12 and 20-25 (description of real-time programmable control architectures); Col. 13, lines 38-40; lines 44-47 (description of a hardwired control context useful for power up situations)].

11. Regarding **claim 3**,

12. DeHon discloses *the reconfigurable integrated circuit of claim 2, wherein the rigid architectures and programmable-rigid architectures have different control fields and control field data widths* [see DeHon, Figs. 1-5; Col. 5, lines 35-42; Examiner's note: DeHon discloses multiple types of architectures (SIMD, MIMD, VLIW, etc) which would have inherently required different control fields and widths.]..

13. Regarding **claim 4,**

14. DeHon discloses *the reconfigurable integrated circuit of claim 1, wherein the first processing element architecture and the second processing element architecture are selected from a plurality of specific architectures, the plurality of architectures including rigid architectures and programmable-rigid architectures* [see DeHon, Fig. 35 and Figs. 1-5; Examiner's note: In Fig. 35, DeHon shows a plurality of functional units (elements 512, 514, and 516) being hardwired to perform either multiply or add functions, thus defining a rigid architecture. However, in Figs. 1-5, DeHon discloses an "ALU" which is routinely configured to perform different operations, similar in spirit to an ALU in a modern processor which is dynamically configured to perform operations dependent on an instruction being processed. These two different architectures thus define two distinct architectures being utilized within the invention disclosed by DeHon.].

15. Regarding **claim 9,**

16. DeHon discloses *the reconfigurable integrated circuit of claim 4, wherein the rigid architectures and programmable-rigid architectures have different control fields and control field data widths* [see DeHon, Figs. 1-5; Col. 5, lines 35-42; Examiner's note: DeHon discloses multiple types of architectures (SIMD, MIMD, VLIW, etc) which would have inherently required different control fields and widths. Furthermore, in Fig. 35, DeHon discloses the use of an 8-bit path (x_i), whereas Fig. 3 shows a 32 bit arrangement.].

17. Regarding **claim 11,**

18. DeHon discloses *the reconfigurable integrated circuit of claim 1, wherein a controller element and processing element are connected using dedicated interconnection means to form a dedicated resource processing element* [see DeHon, Fig. 5; Examiner's note: In Fig. 5, DeHon discloses the use of control elements combined with a processing element (ALU) as an independent dedicated element.].

19. Regarding **claim 12,**

20. DeHon discloses *the reconfigurable integrated circuit of claim 11, wherein a plurality of dedicated resource processing elements are grouped via interconnection means to form a dedicated processing block* [see DeHon, Col. 8, lines 18-21; Examiner's note: DeHon (Col. 8, lines 18 to Col. 9, line 4) discloses an interconnection wear all BPUs and functional units are connected. Thus, it would have been clear that multiple processing elements are connected via reconfigurable interconnect in a system such as that in Fig. 5, where multiple processing elements co-exist within the same fabric of the chip.].

21. Regarding **claim 13,**

22. DeHon discloses *the reconfigurable integrated circuit of claim 1, wherein a controller element and a plurality of processing elements are grouped via interconnection means to form a dedicated resource processing element, the controller element controlling each processing element simultaneously* [see DeHon, Fig. 2; Examiner's note: DeHon discloses a SIMD (single instruction, multiple data) configuration which by definition consists of a controlling element sending data to multiple processors].

23. Regarding **claim 33,**

24. DeHon discloses *the reconfigurable integrated circuit of claim 1, wherein an algorithm that incorporates functions that can be implemented in parallel is directly mapped to corresponding controller elements and processing elements* [see DeHon, Col. 5, lines 49-56], *the processing elements being able to be concatenated dynamically to form different datapath configurations* [see DeHon, Col. 5, lines 35-42], *enabling the algorithm to be implemented in parallel hardware* [see DeHon, Col. 5, lines 49-56; Examiner's note: The above to citations clearly show how DeHon intends for controller and processing elements to be concatenated for different data path configurations. Furthermore, Fig. 5, discloses an MIMD setup which inherently processes data in parallel].

25. Regarding **claim 34,**

26. DeHon discloses *the reconfigurable integrated circuit of claim 1, wherein uniform processing elements can be dynamically concatenated to form larger data width processing elements* [see DeHon, Col. 5, lines 35-42].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-8, 18, 30-32, 39-42, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon in view of Master et al (US Pat. Appl. Pub 2002/0138716; herein referred to as "Master".).

6. Regarding **claim 5,**

7. DeHon discloses the limitations as stated in **claim 4,**

8. DeHon does not disclose the *rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for fixed point arithmetic operations, floating point arithmetic operations, logical operations, shift operations, memory, interfaces, input operations, output operations, bit-level manipulations, combinatorial, synchronous and asynchronous logic.*

9. Master does disclose the *rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for fixed point arithmetic operations, floating point arithmetic operations, logical operations, shift operations, memory, interfaces, input operations, output operations, bit-level manipulations, combinatorial, synchronous and asynchronous logic* [see Master, Para. 0011, lines 5-11; Examiner's note: Although Master does not disclose each function explicitly, it

would have been inherent that the functions disclosed by Master were merely a subset of a larger field of calculations including those disclosed by the applicant.].

10. The advantage of being able to perform the set of functions disclosed by Master would have been to enhance the capabilities of the reconfigurable processor disclosed by DeHon. Obviously, the capability of being able to perform a variety of functions at the functional unit level would improve performance of the system, a universal goal in the art [see Master, Para. 0010, lines 10-16]. This advantage would have motivated one of ordinary skill in the art at the time of invention to enhance the computational abilities of the processor disclosed by DeHon with the set of functions disclosed by Master by simply increasing the instruction set for the processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the ideas of Master and DeHon to increase the performance and capabilities of a reconfigurable processor.

11. Regarding **claim 6**,

12. DeHon discloses the limitations as stated in **claim 4**,

13. DeHon does not disclose *rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for implementing digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions.*

14. Master does disclose *rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for implementing digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions* [see Master, Para. 0012, lines 5-13; Examiner's note: Although Master does not disclose each function explicitly, it would have been inherent that the functions disclosed by Master were merely a subset of a larger field of calculations including those disclosed by the applicant.].

15. The advantage of being able to perform the set of functions disclosed by Master would have been to enhance the capabilities of the reconfigurable processor disclosed by DeHon. Obviously, the capability of being able to perform a variety of functions at the functional unit level would improve performance of the system, a universal goal in the art [see Master, Para. 0010, lines 10-16]. This advantage would have motivated one of ordinary skill in the art at the time of invention to enhance the computational abilities of the processor disclosed by DeHon with the set of functions disclosed by Master by simply increasing the instruction set for the processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the ideas of Master and DeHon to increase the performance and capabilities of a reconfigurable processor.

16. Regarding **claim 7**,

17. DeHon discloses the limitations as stated in **claim 4**,

18. DeHon does not disclose the *programmable-rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for fixed point arithmetic operations, floating point arithmetic operations, logical operations, shift operations, memory, interfaces, input operations, output operations, bit-level manipulations, combinatorial, synchronous and asynchronous logic.*

19. Master does disclose the *rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for fixed point arithmetic operations, floating point arithmetic operations, logical operations, shift operations, memory, interfaces, input operations, output operations, bit-level manipulations, combinatorial, synchronous and asynchronous logic* [see Master, Para. 0011, lines 5-11; Examiner's note: Although Master does not disclose each function explicitly, it would have been inherent that the functions disclosed by Master were merely a subset of a larger field of calculations including those disclosed by the applicant.].

20. The advantage of being able to perform the set of functions disclosed by Master would have been to enhance the capabilities of the reconfigurable processor disclosed by DeHon. Obviously, the capability of being able to perform a variety of functions at the functional unit level would improve performance of the system, a universal goal in the art [see Master, Para. 0010, lines 10-16]. This advantage would have motivated one of ordinary skill in the art at the time of invention to enhance the computational abilities of the processor disclosed by DeHon with the set of functions disclosed by Master by simply increasing the instruction set for the processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the ideas of Master and DeHon to increase the performance and capabilities of a reconfigurable processor.

21. Regarding **claim 8**,

22. DeHon discloses the limitations as stated in **claim 4**,

23. DeHon does not disclose *programmable-rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for implementing digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions.*

24. Master does disclose *rigid architectures* being *selected from a plurality of specific architectures, the plurality of architectures including functions for implementing digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions* [see Master, Para. 0012, lines 5-13; Examiner's note: Although Master does not disclose each function explicitly, it would have been inherent that the functions disclosed by Master were merely a subset of a larger field of calculations including those disclosed by the applicant.].

25. The advantage of being able to perform the set of functions disclosed by Master would have been to enhance the capabilities of the reconfigurable processor disclosed by DeHon. Obviously, the capability of

being able to perform a variety of functions at the functional unit level would improve performance of the system, a universal goal in the art [see Master, Para. 0010, lines 10-16]. This advantage would have motivated one of ordinary skill in the art at the time of invention to enhance the computational abilities of the processor disclosed by DeHon with the set of functions disclosed by Master by simply increasing the instruction set for the processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the ideas of Master and DeHon to increase the performance and capabilities of a reconfigurable processor.

26. Regarding **claim 18,**

27. DeHon discloses the limitations as stated in **claim 11.**

28. DeHon does not explicitly disclose *the dedicated resource elements* [implementing] *digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions.*

29. Master does disclose *the dedicated resource elements* [implementing] *digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions* [see Master, Para. 0012, lines 5-13; Examiner's note: Although Master does not disclose each function explicitly, it would have been inherent that the functions disclosed by Master were merely a subset of a larger field of calculations including those disclosed by the applicant.].

30. The advantage of being able to perform the set of functions disclosed by Master would have been to enhance the capabilities of the reconfigurable processor disclosed by DeHon. Obviously, the capability of being able to perform a variety of functions at the functional unit level would improve performance of the system, a universal goal in the art [see Master, Para. 0010, lines 10-16]. This advantage would have motivated one of ordinary skill in the art at the time of invention to enhance the computational abilities of the processor disclosed by DeHon with the set of functions disclosed by Master by simply increasing the

instruction set for the processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the ideas of Master and DeHon to increase the performance and capabilities of a reconfigurable processor.

31. Regarding **claim 30,**

32. DeHon and Master disclose the limitations as stated in **claim 5**.

33. DeHon also discloses *the logic required to implement each state of a finite state machine is configured dynamically in real time, the selection and configuration of a programmable logic array means being controlled by a vector field output from the current state vector output register* [see DeHon, Col. 14, lines 38-44; Examiner's note: In this citation DeHon discloses a state machine wherein 8 bits of current state output data is returned through a feedback path to the input of the state machine to determine the next state, thus determining in real-time the next state.].

34. Regarding **claim 31,**

35. DeHon and Master disclose the limitations as stated in **claim 5**.

36. DeHon and Master do not explicitly disclose *a plurality of finite state machines are implemented using the same next state memory and programmable logic array means, the current state vector for each finite state machine being stored in separate current state output registers, and individually selectable by enable signal means, the next state memory containing next state vectors for each finite state machine, the address of which if partially formed from an offset address.*

37. However, DeHon does disclose the use of multiple finite state machines (Fig. 29, element 360) for use in gathering input to the processor. Given the customizable aspect of the PLA (Col. 14, lines 33-35), it would have been obvious to one of ordinary skill in the art at the time of invention to utilize only one PLA and to dynamically reconfigure the PLA for a given input. This modification would have reduced the amount of chip utilization substantially and thus would have allowed for more control and processing elements as currently realized. This modification would have caused the use of selectable registers

holding states for inputs and outputs to become obvious, as many similar schemes would have been readily available at the time of invention. Such a scheme similar in spirit would have been similar to the use of instruction cache to hold pending data until a state machine was ready for it. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to minimize chip area consumption by eliminating redundant PLAs since the invention disclosed by DeHon provides a customizable PLA.

38. Regarding **claim 32,**

39. DeHon and Master disclose the limitations as stated in **claim 30.**

40. DeHon also discloses *the programmable logic array means are selected from a plurality of programmable logic array means, the plurality of programmable logic array means including functions for and gates, or gates, nand gates, nor gates, exclusive or gates, invertors, mutliplexers and look-up tables.* [see DeHon, Col. 14, lines 38-45; Examiner's note: DeHon uses an AND and an OR plane, thus selecting from a plurality of logic gates listed in claim 32.].

41. Regarding **claim 39,**

42. DeHon and Master disclose the limitations as stated in **claim 7.**

43. DeHon also discloses *the logic required to implement each state of a finite state machine is configured dynamically in real time, the selection and configuration of a programmable logic array means being controlled by a vector field output from the current state vector output register* [see DeHon, Col. 14, lines 38-44; Examiner's note: In this citation DeHon discloses a state machine wherein 8 bits of current state output data is returned through a feedback path to the input of the state machine to determine the next state, thus determining in real-time the next state.].

44. Regarding **claim 40,**

45. DeHon and Master disclose the limitations as stated in **claim 7.**

46. DeHon and Master do not explicitly disclose *a plurality of finite state machines are implemented using the same next state memory and programmable logic array means, the current state vector for each finite state machine being stored in separate current state output registers, and individually selectable by enable signal means, the next state memory containing next state vectors for each finite state machine, the address of which if partially formed from an offset address.*

47. However, DeHon does disclose the use of multiple finite state machines (Fig. 29, element 360) for use in gathering input to the processor. Given the customizable aspect of the PLA (Col. 14, lines 33-35), it would have been obvious to one of ordinary skill in the art at the time of invention to utilize only one PLA and to dynamically reconfigure the PLA for a given input. This modification would have reduced the amount of chip utilization substantially and thus would have allowed for more control and processing elements as currently realized. This modification would have caused the use of selectable registers holding states for inputs and outputs to become obvious, as many similar schemes would have been readily available at the time of invention. Such a scheme similar in spirit would have been similar to the use of instruction cache to hold pending data until a state machine was ready for it. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to minimize chip area consumption by eliminating redundant PLAs since the invention disclosed by DeHon provides a customizable PLA.

48. Regarding **claim 41**,

49. DeHon and Master disclose the limitations as stated in **claim 39**.

50. DeHon and Master do not explicitly disclose *a plurality of finite state machines are implemented using the same next state memory and programmable logic array means, the current state vector for each finite state machine being stored in separate current state output registers, and individually selectable by enable signal means, the next state memory containing next state vectors for each finite state machine, the address of which if partially formed from an offset address.*

51. However, DeHon does disclose the use of multiple finite state machines (Fig. 29, element 360) for use in gathering input to the processor. Given the customizable aspect of the PLA (Col. 14, lines 33-35), it would have been obvious to one of ordinary skill in the art at the time of invention to utilize only one PLA and to dynamically reconfigure the PLA for a given input. This modification would have reduced the amount of chip utilization substantially and thus would have allowed for more control and processing elements as currently realized. This modification would have caused the use of selectable registers holding states for inputs and outputs to become obvious, as many similar schemes would have been readily available at the time of invention. Such a scheme similar in spirit would have been similar to the use of instruction cache to hold pending data until a state machine was ready for it. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to minimize chip area consumption by eliminating redundant PLAs since the invention disclosed by DeHon provides a customizable PLA.

52. Regarding **claim 42**,

53. DeHon and Master disclose the limitations as stated in **claim 40** (sic).

54. DeHon and Master do not explicitly disclose *a plurality of finite state machines are implemented using the same next state memory and programmable logic array means, the current state vector for each finite state machine being stored in separate current state output registers, and individually selectable by enable signal means, the next state memory containing next state vectors for each finite state machine, the address of which if partially formed from an offset address.*

55. However, DeHon does disclose the use of multiple finite state machines (Fig. 29, element 360) for use in gathering input to the processor. Given the customizable aspect of the PLA (Col. 14, lines 33-35), it would have been obvious to one of ordinary skill in the art at the time of invention to utilize only one PLA and to dynamically reconfigure the PLA for a given input. This modification would have reduced the amount of chip utilization substantially and thus would have allowed for more control and processing

elements as currently realized. This modification would have caused the use of selectable registers holding states for inputs and outputs to become obvious, as many similar schemes would have been readily available at the time of invention. Such a scheme similar in spirit would have been similar to the use of instruction cache to hold pending data until a state machine was ready for it. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to minimize chip area consumption by eliminating redundant PLAs since the invention disclosed by DeHon provides a customizable PLA.

56. Regarding **claim 45**,

57. DeHon discloses the limitations as stated in **claim 13**.

58. DeHon does not explicitly disclose *the dedicated resource elements* [implementing] *digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions.*

59. Master does disclose *the dedicated resource elements* [implementing] *digital filters, Fast Fourier Transforms, Inverse Fourier Transforms, discrete cosine transforms, periodic and non-periodic waveform generation, correlation and convolution functions* [see Master, Para. 0012, lines 5-13; Examiner's note: Although Master does not disclose each function explicitly, it would have been inherent that the functions disclosed by Master were merely a subset of a larger field of calculations including those disclosed by the applicant.].

60. The advantage of being able to perform the set of functions disclosed by Master would have been to enhance the capabilities of the reconfigurable processor disclosed by DeHon. Obviously, the capability of being able to perform a variety of functions at the functional unit level would improve performance of the system, a universal goal in the art [see Master, Para. 0010, lines 10-16]. This advantage would have motivated one of ordinary skill in the art at the time of invention to enhance the computational abilities of the processor disclosed by DeHon with the set of functions disclosed by Master by simply increasing the

instruction set for the processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the ideas of Master and DeHon to increase the performance and capabilities of a reconfigurable processor.

61. Claims 10, 14-17, 19-21, and 36-38 rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon in view of Rupp (US Pat. No. 5,784,636).

62. Regarding **claim 10**,

63. DeHon discloses the limitations as stated in **independent claim 1**.

64. DeHon does not explicitly disclose *a plurality of controller elements and a plurality of processing elements* [being] *grouped via connection means to form a shared resource processing block, the connection means including reconfigurable connection means and dedicated connection means.*

65. Rupp does disclose *a plurality of controller elements and a plurality of processing elements* [being] *grouped via connection means to form a shared resource processing block* [see Rupp, Fig. 2], *the connection means including reconfigurable connection means* [see Rupp, Fig. 2, dashed element between elements 110 and 102; Col. 9, lines 23-26; Examiner's note: The toggle bus between elements 110 and 102 allows for individual RSPs to communicate with other RSPs thus allowing for a reconfigurable connection between any RSP in the system] *and dedicated connection means* [see Rupp, Fig. 2, connections P and Q; Examiner's note: Rupp discloses a dedicated connection between RSPs and the toggle bus (dashed element)].

66. The advantage of configuring controller elements and processing elements in a shared resource configuration would have been to allow greater flexibility in how and what components could be connected within the system [see Rupp, Col. 9, lines 35-40]. This advantage would have been desirable in the environment disclosed by DeHon as DeHon does not explicitly disclose the use of shared controller

elements. By adding shared controller elements, greater flexibility is provided for implementing functions within the system.

67. Regarding **claim 14,**

68. DeHon and Rupp disclose the limitations as stated in **claim 10.**

69. DeHon further discloses *the number of controller elements is greater than the number of processing elements for a particular shared resource block* [see DeHon, Fig. 5 (control elements PC, F, A, B, in relation to one processing element ALU); Col. 5, lines 15-21].

70. Regarding **claim 15,**

71. DeHon does not explicitly disclose *the plurality of processing elements are clocked at a rate that is at least equal to the number of controller elements in a shared resource block.*

72. However, it would have been obvious to one of ordinary skill in the art at the time of invention to clock a number of processing elements faster than a number of controller elements as clock speeds at the time of invention would have been substantially faster than the number of controller elements in a resource block.

73. Regarding **claim 16,**

74. DeHon and Rupp disclose the limitations as stated in **claim 14.**

75. DeHon does not explicitly disclose *the processing elements* [being] *statistically multiplexed between the controller elements.*

76. However, DeHon does disclose the use of two separate control units responsible for controlling the same function within a processing element (Col. 5, lines 19-21). It would have been obvious to one of ordinary skill in the art at the time of invention that if both elements were controlling the same element within a processing element, there would have existed a high probability of corruption of data due to various data hazards. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a multiplexing scheme as to ensure the correct and accurate distribution of control

information to a processing element. By providing a multiplexing scheme, correct functionality and data would have been ensured and would thus increase the performance of the entire invention.

77. Regarding **claim 17**,

78. DeHon and Rupp disclose the invention disclosed in **claim 16**.

79. DeHon does not explicitly disclose *the statistical multiplexing methods* [being] *selected from a plurality of statistical multiplexing methods, the plurality of statistical multiplexing methods including round robin, weighted round robin, request-grant, first-come-first-serve and priority based.*

80. With regards to the arguments made for **claim 16** in this action, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize one of the methods of multiplexing within the limitation of claim 17 upon deciding how to multiplex control signals intended for a processing element. Furthermore, the listed multiplexing methods would have been common in the art at the time of invention and therefore would have been obvious choices upon implementing a multiplexing scheme within the invention disclosed by DeHon.

81. Regarding **claim 19**,

82. DeHon discloses the limitations as stated in **independent claim 1**.

83. DeHon further discloses *the plurality of controller elements and plurality of processing elements are selectively grouped to form a plurality of processing blocks... including dedicated resource blocks* [see DeHon, Fig. 5; Examiner's note: In Fig. 5, DeHon shows controller elements (PC, F, A, B) connected to a processing element (ALU), thus forming a dedicated resource block.]

84. DeHon does not explicitly disclose the resource blocks being *shared resource blocks.*

85. Rupp does disclose the resource blocks being *shared resource blocks* [see Rupp, Fig. 2].

86. The advantage of configuring controller elements and processing elements in a shared resource configuration would have been to allow greater flexibility in how and what components could be connected within the system [see Rupp, Col. 9, lines 35-40]. This advantage would have been desirable

in the environment disclosed by DeHon as DeHon does not explicitly disclose the use of shared controller elements. By adding shared controller elements, greater flexibility is provided for implementing functions within the system.

87. Regarding **claim 20,**

88. DeHon and Rupp disclose the limitations as stated in **claim 19.**

89. DeHon further discloses *reconfigurable interconnection means interconnects a plurality of processing blocks to allow the transfer of control and data information between and among the plurality of processing blocks* [see DeHon, Col. 8, lines 18-21; Examiner's note: DeHon discloses a hierarchical network in this cite that connects all the BFUs, inherently connecting blocks made up of multiple BFUs.].

90. Regarding **claim 21,**

91. DeHon and Rupp disclose the limitations as stated in **claim 20.**

92. DeHon further discloses *the plurality of processing blocks and reconfigurable interconnection means* [being] *arranged to form a hierarchical structure* [see DeHon, Col. 8, lines 18-21; Section 2; Examiner's note: DeHon discloses an architecture consisting of three networks of interconnect. Level 3 including long broadcast lines, level 2 including smaller switchable lines, and level 1 including a smaller neighbourhood mesh. These networks, diminishing in size, constitute a hierarchical structure of communication between processing elements.].

93. Regarding **claim 36,**

94. DeHon discloses the limitations as stated in **independent claim 1.**

95. DeHon does not explicitly disclose *the plurality of controller elements and processing elements* [being] *optimized for implementation in audio applications.*

96. Rupp does disclose *the plurality of controller elements and processing elements* [being] *optimized for implementation in audio applications* [see Rupp, Col. 8, lines 57-63].

97. The advantage for optimizing the processor disclosed by DeHon for use in audio applications would have been to further enhance the performance of the reconfigurable processor in common uses of the processor [see Rupp, Col. 8, lines 51-57]. This advantage would have been desirable in the invention disclosed by DeHon as it would have allowed the invention of DeHon to become a more versatile device capable of performing competitively in different technology areas. Therefore, it would have been obvious to enhance aspects of the device of DeHon to allow for audio applications.

98. Regarding **claim 37**,

99. DeHon discloses the limitations as stated in **independent claim 1**.

100. DeHon does not explicitly disclose *the plurality of controller elements and processing elements* [being] *optimized for implementation in video applications.*

101. Rupp does disclose *the plurality of controller elements and processing elements* [being] *optimized for implementation in video applications* [see Rupp, Col. 8, lines 57-63].

102. The advantage for optimizing the processor disclosed by DeHon for use in video applications would have been to further enhance the performance of the reconfigurable processor in common uses of the processor [see Rupp, Col. 8, lines 51-57]. This advantage would have been desirable in the invention disclosed by DeHon as it would have allowed the invention of DeHon to become a more versatile device capable of performing competitively in different technology areas. Therefore, it would have been obvious to enhance aspects of the device of DeHon to allow for video applications.

103. Regarding **claim 38**,

104. DeHon discloses the limitations as stated in **independent claim 1**.

105. DeHon does not explicitly disclose *the plurality of controller elements and processing elements* [being] *optimized for implementation in telecommunication applications* [see Rupp, Col. 9, lines 47-49].

106. The advantage for optimizing the processor disclosed by DeHon for use in telecommunications applications would have been to further enhance the performance of the reconfigurable processor in

common uses of the processor [see Rupp, Col. 8, lines 51-57]. This advantage would have been desirable in the invention disclosed by DeHon as it would have allowed the invention of DeHon to become a more versatile device capable of performing competitively in different technology areas. Therefore, it would have been obvious to enhance aspects of the device of DeHon to allow for telecommunications applications.

107. Claim 25 and 43-44 rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon in view of Rupp and in view of Master.

108. Regarding **claim 25**,

109. DeHon and Rupp disclose the limitations as stated in **claim 10**.

110. DeHon and Rupp do not disclose *an input to a block or element is dynamically selectable from a group of input signals using de-multiplexer means and an output signal from a block or element is dynamically selectable from a group of output signals using multiplexer means, the de-multiplexer and multiplexer being controlled by a reconfigurable interconnect controller or controller element.*

111. Master does disclose *an input to a block or element is dynamically selectable from a group of input signals using de-multiplexer means* [see Master, Fig. 4, element 280] *and an output signal from a block or element is dynamically selectable from a group of output signals using multiplexer means* [see Master, Fig. 4, element 290], *the de-multiplexer and multiplexer being controlled by a reconfigurable interconnect controller or controller element* [see Master, Para. 0049].

112. The advantage of using multiplexing and demultiplexing for a block within a reconfigurable processor would have been to ensure the correct selection of inputs and outputs upon receiving data to be processed [see Master, Para. 0048, lines 7-14]. This advantage would have been desirable in the invention disclosed by DeHon as it would have allowed for the appropriate routing of signals to the appropriate processing elements, an aspect not explicitly discussed by DeHon.

113. Regarding **claim 43**,

114. DeHon and Rupp disclose the limitations as stated in **claim 12**.

115. DeHon and Rupp do not disclose *an input to a block or element is dynamically selectable from a group of input signals using de-multiplexer means and an output signal from a block or element is dynamically selectable from a group of output signals using multiplexer means, the de-multiplexer and multiplexer being controlled by a reconfigurable interconnect controller or controller element.*

116. Master does disclose *an input to a block or element is dynamically selectable from a group of input signals using de-multiplexer means* [see Master, Fig. 4, element 280] *and an output signal from a block or element is dynamically selectable from a group of output signals using multiplexer means* [see Master, Fig. 4, element 290], *the de-multiplexer and multiplexer being controlled by a reconfigurable interconnect controller or controller element* [see Master, Para. 0049].

117. The advantage of using multiplexing and demultiplexing for a block within a reconfigurable processor would have been to ensure the correct selection of inputs and outputs upon receiving data to be processed [see Master, Para. 0048, lines 7-14]. This advantage would have been desirable in the invention disclosed by DeHon as it would have allowed for the appropriate routing of signals to the appropriate processing elements, an aspect not explicitly discussed by DeHon.

118. Regarding **claim 44**,

119. DeHon and Rupp disclose the limitations as stated in **claim 13**.

120. DeHon and Rupp do not disclose *an input to a block or element is dynamically selectable from a group of input signals using de-multiplexer means and an output signal from a block or element is dynamically selectable from a group of output signals using multiplexer means, the de-multiplexer and multiplexer being controlled by a reconfigurable interconnect controller or controller element.*

121. Master does disclose *an input to a block or element is dynamically selectable from a group of input signals using de-multiplexer means* [see Master, Fig. 4, element 280] *and an output signal from a*

block or element is dynamically selectable from a group of output signals using multiplexer means [see Master, Fig. 4, element 290], *the de-multiplexer and multiplexer being controlled by a reconfigurable interconnect controller or controller element* [see Master, Para. 0049].

122. The advantage of using multiplexing and demultiplexing for a block within a reconfigurable processor would have been to ensure the correct selection of inputs and outputs upon receiving data to be processed [see Master, Para. 0048, lines 7-14]. This advantage would have been desirable in the invention disclosed by DeHon as it would have allowed for the appropriate routing of signals to the appropriate processing elements, an aspect not explicitly discussed by DeHon.

123. Claims 23-24, 26-29, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon in view of Mirsky et al. (US Pat. No. 5,915,123; herein referred to as Mirsky).

124. Regarding **claim 23,**

125. DeHon discloses the limitations as stated in **independent claim 1**.

126. DeHon does not explicitly disclose *signal routing* [being] *controlled by one or a plurality of reconfigurable interconnect controllers and one or a plurality of controller elements, the reconfigurable interconnect controllers and controller elements having memory means to store one or a plurality of routing configurations.*

127. Mirsky does disclose *signal routing* [being] *controlled by one or a plurality of reconfigurable interconnect controllers* [see Mirsky, Fig. 7, element 1006; Col. 7, lines 35-38] *and one or a plurality of controller elements* [see Mirsky, Fig. 2, element 214], *the reconfigurable interconnect controllers and controller elements having memory means to store one or a plurality of routing configurations* [see Mirsky, Col. 7, lines 13-16 (reconfigurable interconnect memory); Col. 5, lines 8-14 (controller element memories)].

128. The advantage of using a hierarchal configuration of controller elements (reconfigurable interconnect controllers above controller elements) would have been to allow for a more efficient transfer of configuration data to an entire system. By allowing for a fast transfer of configuration data to a higher hierarchal controller (via a higher interconnect level such as level 3 disclosed by DeHon) and using a lower-level local network to distribute said data to individual controller elements, one would have been able to enhance the speed at which a processor operates, thus increasing performance. This advantage would have been desirable in the invention of DeHon as it would have increased the performance as stated, which would have been a common obvious goal in the art at the time of invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the hierarchal structure disclosed by Mirsky in the invention disclosed by DeHon.

129. Regarding **claim 24**,

130. DeHon and Mirsky disclose the limitations as stated in **claim 23**.

131. DeHon and Mirsky do not explicitly disclose *one signal line* [being] *connected electrically to another signal line using a pass transistor, the pass transistor or a group of pass transistors being controlled by an individual output from a reconfigurable interconnect controller or a controller element.*

132. However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a pass transistor to control the routing of control signals throughout a reconfigurable processor. At the time of invention, it would have been common knowledge that a pass transistor is the most efficient and economical way to route electrical signals on a processor. Thus, one of ordinary skill in the art would have been motivated to utilize a simple switching structure, such as a pass transistor, to control the routing of signals within the reconfigurable circuit disclosed by DeHon and Mirsky.

133. Regarding **claim 26**,

134. DeHon discloses the limitations as stated in **independent claim 1**.

135. DeHon also discloses *the transfers being dynamically operable in real time* [see DeHon, Col. 12, lines 7-15; Examiner's note: In this passage, DeHon describes the BFUs reconfiguring each other dynamically, thus in real time.] *and non real time* [see DeHon, Col. 13, lines 43-47; Examiner's note: In this passage, DeHon discloses a plurality of connections be configured, such as in a startup mode, thus not in real time.].

136. DeHon does not explicitly disclose *master controller means* [being] *provided to transfer configuration data to one or a plurality of micro-code memories and one or a plurality of reconfigurable interconnect memories.*

137. Mirsky does disclose *master controller means* [being] *provided* [see Mirsky, Fig. 7, element 1004] *to transfer configuration data* [see Mirsky, Col. 7, lines 16-18] *to one or a plurality of micro-code memories* [see Mirsky, Col. 7, lines 35-38; Examiner's note: Mirsky does not explicitly use the terminology "micro-code", however, the function of the CNI unit is to reconfigure a selected group of functional units by re-routing the interconnect which is analogous with the function of a microcode memory.] *and one or a plurality of reconfigurable interconnect memories* [see Mirsky, Col. 5, lines 8-11; Examiner's note: Mirsky discloses configuration memories located in the BFUs further coupled to the CNI (Col. 5, lines 11-14), thus receiving configuration information from the CNIs to be stored in local configuration memories.].

138. The advantage of having a master controller to transfer configuration data would have been to allow for a more organized control structure, wherein the user need only provide one overall configuration instead of multiple smaller configuration files. This scheme would have been favorable in the invention disclosed by DeHon, as it would have provided for a more structured and intuitive configuration interface for a user of the system.

139. Regarding **claim 27**,

140. DeHon and Mirsky disclose the limitations as stated in **claim 26**.

141. Mirsky further discloses *the master controller means* [being] *formed from one or plurality of processing blocks* [see Mirsky, Col. 4, lines 36-38; Examiner's note: Mirsky discloses processing elements being created from MCPE building blocks, thus DeHon enables one of ordinary skill to create the CNS master controller out of MCPE building blocks.].

142. Regarding **claim 28,**

143. DeHon and Mirsky disclose the limitations as stated in **claim 26.**

144. Mirsky further discloses *the master controller means* [being] *an embedded processor* [see Mirsky, Col. 4, lines 45-47; Examiner's note: Mirsky discloses a method of using external hardware for performing more sophisticated instructions, therefore DeHon enables on of ordinary skill in the art to utilize an additional processor if one of ordinary skill would have determined the master processor too complex to be comprised of MCPEs.].

145. Regarding **claim 29,**

146. DeHon and Mirsky disclose the limitations as stated in **claim 26.**

147. Mirsky further discloses *the master controller means* [being] *an external controller means* [see Mirsky, Col. 4, lines 55-67 (with attention to lines 62-63); Examiner's note: Mirsky discloses a master control block (which is a different entity from the CNS) which is a level above the CNS controller which performs the master controller activities as claimed by the applicant.].

148. Regarding **claim 35,**

149. DeHon discloses the limitations as stated in **independent claim 1.**

150. DeHon and Mirsky do not explicitly disclose *one or a plurality of controller element and processing elements are initially configured to implement test logic to test the remaining controller and processing elements, any fault conditions being reported to a master controller so the faulty elements can be excluded from implementing live and operational circuits.*

151. However, Mirsky discloses the use of the JTAG architecture within the environment of a reconfigurable circuit (Col. 4, lines 55-67). It would have been obvious to one of ordinary skill in the art at the time of invention that the inclusion of JTAG capabilities would have been to test elements in the reconfigurable processor, as the JTAG architecture is commonly used to test blocks within processors. Furthermore, the JTAG architecture would have allowed for an in-circuit debugging capability which would have allowed one of ordinary skill in the art at the time of invention to disable faulty elements during runtime. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the JTAG interface disclosed by Mirsky within the invention disclosed by DeHon.

152. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon in view of Rupp and Mirsky.

153. Regarding **claim 22**,

154. DeHon and Rupp disclose the limitations of **claim 20**.

155. DeHon and Rupp do not explicitly disclose *the plurality of processing blocks and reconfigurable interconnection means...arranged to form a fractal structure.*

156. Mirsky does disclose *the plurality of processing blocks and reconfigurable interconnection means...arranged to form a fractal structure* [see Mirsky, Fig. 7].

157. The advantage of using a fractal structure as disclosed by Mirsky would have been to minimize the amount of time required to load configuration data into the individual processing elements [see Mirsky, Col. 7, lines 20-22]. By using a fractal structure, the data would be able to sent on a fast, global network to individual child controllers which could then in turn utilize the faster local interconnects to distribute the configuration information. This advantage would have been desirable in the invention disclosed by DeHon as it would have improved the speed of the processor by considerably minimizing the amount of time required for a configuration setting to be received by the processing elements from a

source. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a fractal structure when organizing the processing elements of DeHon.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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